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ORGINAL ARTICLE

The Effect of Gate Length on SOI-MOSFETs Operation

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ABSTRACT

The effect of gate length on the operation of silicon-on-insulator (SOI) MOSFET structure with a layer of buried silicon oxide added to isolate the device body has been simulated. Three transistors with gate lengths of 100, 200 and 500 nm are simulated. Simulations show that with a fixed channel length, when the gate length is increased, the output drain current characteristics slope is increased, and therefore the transistor transconductance increases. Moreover, with increasing the gate length, the effect of the drain voltage on the drain current is reduced, which results in the reduced drain induced barrier lowering.

***KEYWORDS**: SOI-MOSFET, silicon, transconductance, drain voltage.*

INTRODUCTION

The demand for faster and cheaper microelectronic devices has led to an incredible shrinking of devices and a corresponding increase in component density. This modern technology brings with it some difficult problems of heat transfer. Thermal power is produced at many device junctions, and the heat needs to diffuse away from the components, or the devices would suffer from self-heating heating effects, including degradation of reliability and electronic performance. Some of these junctions involve appreciable power dissipation. The oxide of silicon-on-insulator (SOI) structure has a very low thermal conductivity of approximately 1.4W/m/K, which may be compared with values near 100W/m/K in bulk silicon [1]. Due to the fact that the oxide is buried between the silicon device body and silicon substrate, self-heating in such SOI structure is substantially enhanced.

SOI–MOSFET transistors have been found to be more effective than ordinary transistors made from the semiconductor materials [1-2]. In SOI-MOSFETs the forming layer of the transistor channel is very thin and the sub-base current is also zero because of their insulation. Hence, carriers are closer to the gate, so the gate will have a greater control over the channel current. In SOI transistors, the effect of drain voltage on threshold voltage is less than that of the transistors made in the semiconductor part [3]. SOI transistors will replace the commonly used transistors in the future, for their benefits.

To investigate the operation of SOI transistors, analytical and simulation methods were studied [4-5]. However, the operation of them have not been fully identified, and further research is needed.

In this study, a few thin SOI transistors were investigated. The channel length was held constant, but the gate length covers part or all of the channel. Then by holding the channel length constant, the effect of the change of the gate length on the characteristics of the transistor was studied. It has been indicated that in nano transistors made with carbonic nano pipes if the gate connection does not cover a part of the channel, some characteristics of the transistor will improve [6-7]. In this study, a nano transistor made of silicon was used. Stimulation for three transistors with gate lengths of 100, 200, 500 nm were carried out.

This article is organized as follows. Details of the simulation methods are presented in section 2, and the results of the change in gate length on the gate current-voltage curve with regard to different drain voltages, and the comparison of threshold voltage are presented in section 3. In section 4 the results of the stimulation for the comparison of the drain current-voltage curve with regard to the different gate voltages are proposed.

II- SIMULATION MODEL

We have supposed three SOI-MOSFETs with 500, 200 and 100 nm gate lengths in the simulation. The simulated device can be described simply by three regions (figure 1), representing source and drain doping implants and a central region containing the supply layers. The field cell size used for

the central region is 40 nm^2 (horizontal×vertical), but that in the high doped source and drain implants is finer (10 nm^2).

Figure 1 shows a schematic of the modelled SOI- MOSFET. The source and drain have ohmic contacts and gate is in Schottky contact in 1 eV to represent the contact potential at Au/Pt. The source and drain regions are doped to 2×10^{24} m^{-3} electron concentration and the top and down buffer layers are doped to 2×10^{23} m^{-3} and 5×10^{22} m^{-3} concentration, respectively. The channel thickness is about 50 nm and the gate oxide layer has 20 nm thickness. The balance equations are carried out to simulate electron transport properties in the device.

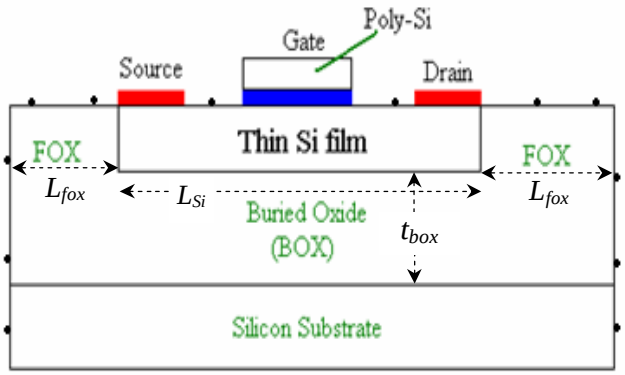


Figure 1: Simplified SOI Structure

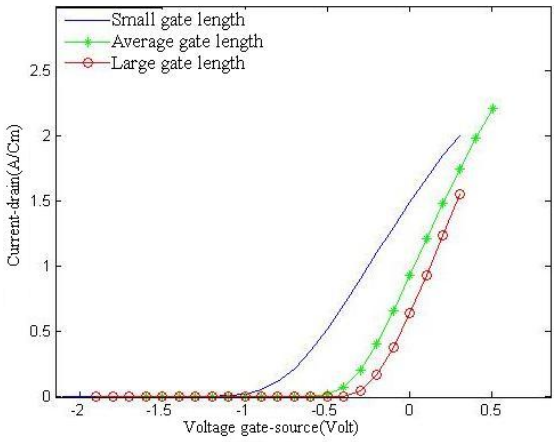
III- CALCULATION RESULTS

Figure 1 shows gate current-voltage carve with drain voltage 0.2 and 2 volts in 3 different gate length cases (small, average and large) and channel length is 500 nm. In these figures see that increscent of gate length increasing slope of I-V carve and g_m. Other hand with different gate voltage, drain current for smaller gate length more than other tows.

In this case modulation of channel gate length is big and makes large increment drain current.

Figures 3 and 4 show carves of gate current-voltage with drain voltage 0.2 volt and transistor have 200 and 100 nm lengths. Because studying DIBL effect, threshold voltages for 3 cases with different drain voltage have been presented. So, we see whatever gate length is more, gate control increase on channel and drain voltage effect less on drain current and other word DIBL decrease.

By comparing results in different 3 cases, we conclude that increment of gate length, slope of I_D-V_{GS} carve for 500 nm gate length more than 200 and 100 nm gate lengths and other hand drain voltage effect on drain current for 500 nm gate length less than 100 and 200 nm.



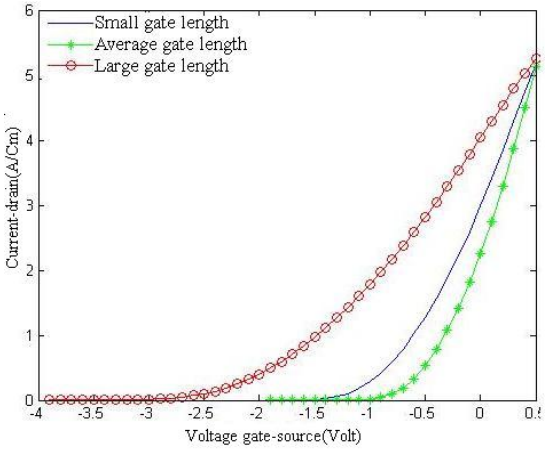


Figure 2: Current drain as a function of voltage gate-source with drain voltage 2 V and different gate length small, average and large and transistor 100 nm lengths.

Figure 2 shows drain-source voltage for 3 cases, small gate length, average and large gate length and transistor have 500 nm gate length. We see, increment of gate length increase gate length control on channel current. So, drain voltage has lesser effect on current then outing resistant of transistor increase. For more comparing, simulation results of transistor with gate length in tow cases, small and large, have been showed in figures 8 and 9. We see again, increment of gate length, drain voltage have lesser effect on current but more than previous case.

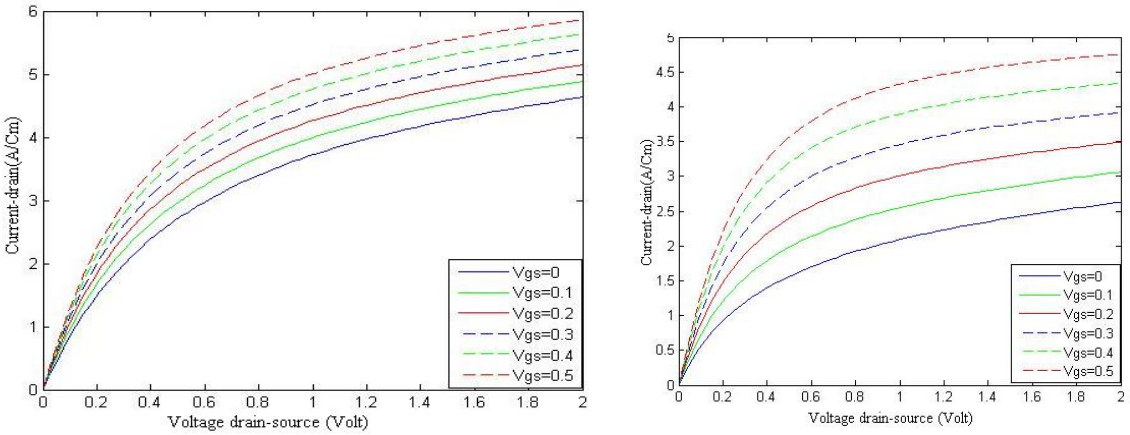


Figure 3&4: Current drain as a function of drain-source voltage with varies gate-source and small gate length and transistor have 500 nm gate length.

CONCLUSION

In this paper gate length effect in SOI-MOSFET transistor has been studied. It is seen that whatever gate length is increased then the slope of output I-V characteristics is increased that confirmed an increment of current and transitional conduction of transistor. Also, increasing of gate length increase gate control on channel current and drain voltage have lesser effect on current. This causes the resistant of transistor will be increased.

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